IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of manufacturing a semiconductor device having a dielectric capacitor including a bottom electrode, a dielectric layer and a top electrode on an underlying substrate having a three-dimensional structure, comprising:

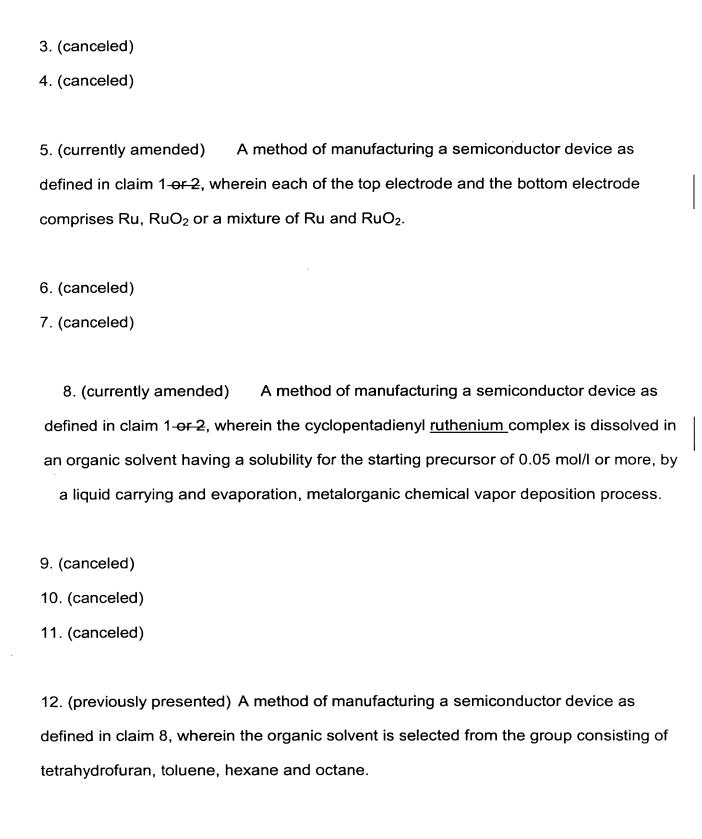
providing a substrate having an insulation layer provided thereon, the insulation layer having a hole formed therein;

forming a bottom electrode on at least a side wall of the insulation layer in the hole;

providing a dielectric layer on the bottom electrode; and forming a top electrode on the dielectric layer;

wherein the bottom electrode and the top electrode are formed by a metalorganic chemical vapor deposition process at 180°C or higher and 250°C or lower using a cyclopentadienyl <u>ruthenium</u> complex as a precursor <u>and a reaction gas selected</u> from the group consisting of O₂, H₂, N₂O, O₃, CO and CO₂, where a volume ratio of the reaction gas to a carrier gas is 1% or more.

2. (currently amended) A method of manufacturing a semiconductor device as defined in claim 1, wherein one of O_2 ,[[H₂,]] N_2O , O_3 , CO and CO_2 is used as a reaction gas and the volume ratio of the reaction gas to a carrier gas is 1% or more.



- 13. (canceled)
- 14. (canceled)
- 15. (previously presented) A method of manufacturing a semiconductor device as defined in claim 1, wherein said dielectric layer is formed by a metalorganic chemical vapor deposition process.
- 16. (previously presented) A method of manufacturing a semiconductor device as defined in claim 1, wherein the bottom electrode is formed homogenously on the side wall of the insulation layer in the hole and on the bottom of the hole.
- 17. (previously presented) A method of manufacturing a semiconductor device as defined in claim 16, wherein the hole has an aspect ratio of depth/diameter of 3 or more.